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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/817,448
Filing Date: April 02, 2004
Appellant(s): FLOMAN ET AL.

Anatoly Frenkel #54106
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 12/12/2007 appealing from the Office action mailed 5/7/2007.

(1) Real Party in interest

A statement identifying by name the real party interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The statement of the status of Amendments After Final contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal has minor typographic errors as follows,

The Ganton reference should be US Pub 2003/0163656.

The Lin reference should be US 7032105.

The Eaton et al. reference should be US Pub 2005/0128322.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US Pub 2005/0128322	Eaton et al	6-2005.
US Pub 2003/0163656	Ganton, Robert Bruce	8-2003.
US 7032105	Lin, I-Ming	6-2004.

US 7093153	Witek et al	8-2006.
US 2005/0041473	Pua et al	2-2005.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4,8,12,20-22, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (US Pub 2003/963656), in view of Lin (US 7032105) and further in view of Eaton et al (2005/0128322).

As in claim 1, Ganton discloses a memory module comprising: a fast nonvolatile random access memory, responsive to a command/data signal provided by a processor (Ganton's Fig 1 discloses a fast non-volatile random access memory, in which data in #115 loading into RAM #120 responsive to processor CPU using a command address data signals, see Ganton's paragraphs 11, 29; Ganton further discloses the memory #115), configured to provide a

permanent storage of information before said command/data signal is provided, configured to execute a command comprised in said command/data signal using said permanently stored information (Ganton's paragraph 25 non-volatile memory provides storages for operating systems, program code, applications, radio calibration parameters and phone books information, Ganton's paragraph 30 further discloses executing using code permanently stored in the non-volatile random access memory), for providing a direct communication between said non-volatile random access memory and the processor (Ganton's Fig 1, command address/data signal providing direct communication between non-volatile memory and processor); and

Ganton does not expressly disclose a double interface configured to communicate with said processor. Ganton discloses the memory controller includes well known in the art convert circuitry to converting different protocol for interfaces with different memory devices such as non-volatile, sram, sdram etc.. Ganton further discloses using different clock edges to convert and clocking data in different memory interfaces. Ganton does not expressly disclose the double rate DDR type interface. However, Lin discloses a memory controller having SDRAM and DDR interface conversion circuitry (Lin's column 4 lines 35-39, Fig 1: #74). It would have been obvious to one of ordinary skill in the art at the time of invention to include conversion circuit and the memory storing method as suggested by Lin in Ganton's system to convert load/store commands issued by the CPU into appropriate memory access commands for accessing DDR dynamic random memory, thereby providing the system with a fast efficient method to store data into DDR DRAM in a permanent manner, see Lin's column 3 lines 57-67; Lin's column 3 lines 57-62 further discloses a mechanism wherein a memory device, for example Lin's Fig 3: #68

SDRAM, readily to be a non-volatile memory by having an uninterruptible power supply (i.e battery)),

Ganton and Lin do not expressly disclose the claim's aspect of electronic device's parts. However, Eaton discloses an electronic device (Eaton's paragraph 1, cellular phone, PDA etc..) capable of combining several parts including memory module part (Eaton's Fig 2: #144 paragraph 15 hierarchical memory in mobile device, ROM EEPROM RAM etc..) processor part (Eaton's Fig 2: #152), speaker part (Eaton's Fig 2: #156). It would have been obvious to one of ordinary skill in the art at the time of invention to include the method of combining parts in an electronic device as suggested by Eaton in Ganton's system modified by Lin which operates parts in a combination manner, thereby further providing new features while maintain the small size and portability of the electronic device (Eaton's paragraph 2).

As in claim 2, Ganton discloses the memory controller having converting circuitry to convert different protocols for interfacing with different memory devices such as non-volatile, sram, sdram etc.. Ganton further discloses of using different clock edges to convert and clocking data in different memory interfaces. Ganton does not expressly disclose the double rate DDR type interface. However, Lin discloses a memory controller having SDRAM and DDR interface conversion circuitry (Lin's column 4 lines 35-39, Fig 1: #74). It would have been obvious to one of ordinary skill in the art at the time of invention to include conversion circuit and the memory storing method as suggested by Lin in Ganton's system to convert load/store commands issued by the CPU into appropriate memory access commands for accessing DDR dynamic random memory, thereby providing the system with a fast efficient method to store data into DDR DRAM in a permanent manner, see Lin's column 3 lines 57-67).

As in claims 3-4, wherein the fast non-volatile random access memory is configured to provided a temporal storage of data (claim 3, Ganton's paragraph 28 discloses non-volatile random access memory stores temporary data such as recent call lists); wherein said fast non-volatile random access memory comprises an information storage area configured to permanently store said information; and a temporal data storage area for the temporal storage of said data (claim 4, Ganton's paragraph 28 discloses the non-volatile storage stores permanently information such as operating system and temporary data such as phone book, recent call lists, and a temporal data storage area/memory configured to store said data, Ganton's paragraph 28 lines 3-15. Note that SDRAM is readily a non-volatile memory by having a non-interrupt power source, see Lin's Fig 3: #68 SDRAM).

As in claim 8, Ganton discloses wherein said information comprises an application program for operating an electronic device (Ganton's paragraph 25 discloses information comprises program codes, applications, radio calibration parameters and phonebook information).

Claim 12 rejected based on the same rationale as of claim 2.

Claim 20 rejected based on the same rationale as of claim 1.

As in claims 21-22, Ganton discloses a power and reset block, for resetting said processor and for resetting said fast non-volatile random access memory; wherein said electronic device is a portable electronic device, a mobile electronic device or a mobile phone (claim 21, power supplying and resetting circuitry for a system is represented in Ganton's Fig 7: #26, paragraph 4 the device is a mobile phone etc..).

Claim 33 rejected based on the same rationale as of claim 1

Claims 5,7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (2003/0163656), Lin (US 7032105), Eaton et al (2005/0128322) as applied to claim 4 and in view of Witek et al (US 7093153).

As in claim 5, Ganton, Lin, and Eaton do not expressly disclose at least one register for setting operating parameters of the fast non-volatile random access memory or to protect said data or said information during said execution. However, Witek discloses a controller having set of registers configured to set operating parameters of the memory devices such as sdram, sram, and non-volatile memory devices (Witek's column 5 lines 40-65). It would have been obvious to one of ordinary skill in the art at the time of invention to include registers sets in memory controllers as suggested by Witek in Ganton's system modified by Lin and Eaton to allow hardware logic to optimize the memory devices operation dynamically in an efficiently manner, thereby to further reduce the power consumption of the overall system (Witek's column 2 lines 1-10). Witek's column 5 lines 55-64 further discloses the set of register (i.e address region control registers) are used to protect write to a region, for example write to a read only region will be protected.

As in claim 7, Witek's column 5 lines 55-64 further discloses the set of register (i.e address region control registers) are used to protect write to a region, for example writing to a read only region will not be allowed (i.e write protection).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (2003/0163656), Lin (US 7032105), Eaton et al (2005/0128322), Witek et al (US 7093153) as applied to claim 5 and in view of Micron (Micron's synchronous DRAM 256Mb: x4, x8, x16 SDRAM features)

As in claim 6, Witek further discloses wherein said operating parameters comprises at least one of timings for a particular frequency, and frequency ranges with a corresponding core voltage range (Witek's Fig 1 discloses a phase lock loop logic provides timing for a particular frequency, and providing clocks in a range of frequencies. Witek's column 6 lines 8-50 further discloses the operating parameters are used to optimizing the devices' operating frequencies corresponding to the core voltages being used in the devices, thus the overall power consumption of the system can be reduced). None of Ganton, Lin, Eaton and Witek expressly discloses the frequency ranges corresponding to a core voltage for a memory. However, Micron's page 1, table 2 discloses any memory device with a core frequency capable of operating in a range of frequencies. For example, Table 2: a memory device having an operating frequency ranges 167 MHz to 100 Mhz corresponding to a core voltage for a memory device. It would have been obvious to one of ordinary skill in the art at the time of invention to provide frequency ranges information corresponding to a core voltage of a memory device as suggested by Micron in Ganton's system thereby further allowing the system to optimize the data throughput accordingly to the frequency ranges of the memory device (see Micron's table 2).

Claims 9-11,13-18,34 rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (2003/0163656), Lin (US 7032105) and Eaton et al (2005/0128322) as applied to claim 1, and in view of Pua et al (US 2005/0041473).

As in claim 9, Ganton, Lin and Eaton do not expressly disclose the claim's detail of a mass memory, However, Pua's Fig 2 discloses a memory controller (Pua's Fig 2: #12 controlling IC) comprises a mass memory configured to provide (memory attaching to the Fig 2:

#131 NAND IC terminal) more storages to store information in response to a command/information signal from the memory controlling integrate circuitry Fig 2: #12 IC (see Pua's paragraph 20 lines 13-16). It would have been obvious to one of ordinary skill in the art at the time of invention to include memory controller capable of controlling multiples memory devices as suggested by Pua in Ganton's system modified by Lin and Eaton, thereby extra memory capacity can be readily added in the system (Pua's paragraph 20 lines 13-16). Similarly, Ganton further discloses that an application-specific integrate circuit is employed to provide command/information signal to memory device (Ganton's Fig 5, paragraph 33).

As in claim 10, Pua's Fig 2 discloses wherein said further information is provided to say fast non-volatile random access memory (information of memory attaching to Pua's Fig 2: #131 is provided to non-volatile memory Fig 2: #13).

As in claim 11, Pua discloses information in the extend memory attached to Pua's Fig 2: #131, is provided to the non-volatile random access memory (Pua's Fig 2: #13), this information will be used/processed by the processing element (Ganton's Fig 5: #525,paragraph 34). Ganton further discloses that the memory area, Ganton's Fig 1: #120 is configured to execute a further command comprises in said command/data signal using said further information, for example information in Ganton's Fig 1: #115 memory area).

As in claim 13, Ganton discloses a non-volatile random access memory integrate circuit package comprises the application specific integration circuit (Ganton's Fig 1: #105, serial memory interface controller), the mass memory and the fast non-volatile random access memory (Ganton's Fig 1: #115), Pua further disclose a mass memory readily attached to the system to increase the total capacity of the memory system (memory attached to Pua's Fig 2: #131) or the

application specific integration circuit (Ganton's Fig 1: #105, serial memory interface controller), and the fast non-volatile random access memory (Ganton's Fig 1: #115), or the mass memory and the non-volatile random access memory (Ganton Fig 3, paragraph 31, discloses another embodiment in which the processor having extra circuitry to provide reading/processing boot code in the onboard ROM Fig 1: #307, thus the circuitry in the memory interface (Fig 3: #310) is reduced to merely carrying out the command/data from the processor (Fig 3: CPU)).

As in claim 14, Pua discloses the memory controller (Pua's #12) comprises multiples memory interfaces (Fig 1: #15 I/O interface, #16 memory card interface, #17 memory interface, and memory IC #14) configured to provide additional storage/ memory to the system. Pua does not expressly disclose additional storage/memory as a dynamic random access memory, however, using the dynamic random access memory for storage has been known in the art (see Ganton's paragraph 28 lines 8-11).

Claim 15 rejected based on the same rationale as in claim 13 and 14.

As in claim 16, Ganton discloses the dynamic random access memory is loaded with code (images is stored in SDRAM); this code is readily for used by the CPU. Ganton's paragraph 28 further discloses that the memory controller use the memory in the system in a hierarchical manner. For example, data being paged from/to memory Fig 1: #120 and memory Fig 1: #115).

As in claim 17, Pua discloses removable mass memory (memory attaching to Fig 2: #131 nand ic terminal, #1411 sram ic terminal) provided further information to the fast non-volatile random access memory (Pua's Fig 2: #13) or to sram IC #141 or to both #13 and #141 in response to a further command/information signal provides by the application specific integration circuit (Pua's Fig 2: #12 control IC). Although Pua does not expressly disclose the

extend memory sram IC #141 can be a dynamic random access memory. However, a dynamic random access memory can readily be used to extend memory capacity in the system as disclosed by Ganton's paragraph 28 lines 8-11.

As in claim 18, the claim rejected based on the same rationale of claims 14 and 17. Ganton's paragraph 28 further discloses that the memory controller use the memory in the system in a hierarchical manner. For example, data being paged from/to memory Fig 1: #120 and memory Fig 1: #115).

As in claim 34, Pua further discloses the circuitry is integrated into a module (Pua's paragraph 7).

Claim 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Ganton (2003/0163656), Lin (US 7032105) and Eaton et al (2005/0128322) as applied to claim 1, and in view of Coufal et al (IBM Technical Disclosure Bulletin, Vol 37 No. 11 November 1994, pp 421-424).

As in claim 19, Ganton,Lin, and Eaton do not expressly disclose the fast non-volatile random access memory is a magneto-resistive random access memory, a ferroelectric random access memory, or an Ovonic memory type. However, Coufal discloses a non-volatile random access memory is build as a ferroelectric random access memory (Coufal's first paragraph). It would have been obvious to one of ordinary skill in the art at the time of invention to include a ferroelectric random access memory by Coufal in Ganton's system modified by Lin and Eaton thereby further providing a fast non-volatile random access memory with a huge memory capacity (Coufal's first paragraph, fast access time, and high memory density, third paragraph).

(10) Response to Argument

Appellant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Appellant's arguments for the following reasons:

A) Appellant arguments regarding the rejection of claim 1 under 35 USC 103(a) are not persuasive.

Appellant main argument is that the recited prior art teaching of an DRAM memory equipped with a battery is not the "**non-volatile random access memory**" recited in claim 1 and alleging that such memory is "technically wrong". Examiner disagrees. Appellant admitted that " **by definition, the non-volatile memories are characterized by their ability to retain the stored data even when the power is interrupted**" for example, when a main power source temporary fails (Appeal brief's page 12 lines 1-6,dated 12/12/07). That is exactly a DRAM memory equipped with a battery would be. There isn't any "technically wrong" with having DRAM memory equipped with battery to provide and retain the stored data when the power is interrupted. In fact, such memory is well known in the art as "non-volatile random access memory" and clearly defined in The Microsoft Computer Dictionary fifth edition 2002, which states "NVRAM Acronym for non volatile random access memory. Non-volatile memory read/write memory or **normally volatile memory that has been fitted with a battery backup to retain data**".

Appellant further argues that "using additional battery power for maintaining permanent "non-volatile" status of the volatile memory would not make any practical sense, therefore a

person skill in the art would not be further motivated..to incorporate Lin into Ganton..". Examiner disagrees. A portable device such as, cell phones, PDA, or laptop computer is equipped with battery to supply power to components inside such as processors, memory devices, in addition to the power source from a power line. Because the battery inherently designed in such portable devices for supplying power. It would be obvious to one skill in the art to use the battery to supply internal memory devices such as DRAM thereby to provide the system with a faster, higher density memory and also capable of retaining data.

Regarding Appellant's argument "the memory 144 of Eaton et al..is different from the memory module of 25.. of the present invention which has much greater capabilities then the memory 144 of Eaton….In other words, if the memory 152 of Eaton et al would .have the baseband and capacities of the memory module 25 described in the present invention, then the size of the memory 152 would be practical unacceptable to use it in a camera phone 100..", Examiner disagrees.

It's noted that in Eaton, there is not memory 152, thus Examiner interprets that Applicant's argument "..memory 152 of Eaton.." recited above, intent to be "Eaton's memory 144".

Eaton's paragraph 15 teaches the memory 144 represents a hierarchical of memory devices typically being used in the portable device which can be RAM, ROM, DRAM..), wherein DRAM memory provides large amount of storage with small foot print readily to be incorporated in any electronic device. Therefore Eaton's teaching of using hierarchical memory devices in the portable device meets the claim's recitation "said memory module and said processor are parts of an electronic device".

Regarding Appellant's arguments that it's not possible to substitute one type of memory with another in the memories of recited prior art. Examiner disagrees, simply because it's known in the art to have different memory devices/types in a system. And depending of the system's specific criteria, a different memory device can be substituted to achieve the goal. For example, when a design requires a large amount of memory and small foot print device, a low density type memory RAM device would be replaced/substituted by a high density memory such as DRAM device, or a "volatile random access memory" type device could be replaced/substituted with a "non-volatile random access memory" type device when a design requires data to be retained in the memory regardless of power interruption.

Thus, additionally, the claim would have been obvious because the substitution of one known element for another would have yielded predicable results to one of ordinary skill in the art at the time of the invention. In this instant, the substitution of one memory type for another would be obvious because substituting "volatile random access memory" with a "non-volatile random access memory" would have yield predictable results, retaining data, to one of ordinary skill in the art at the time of the invention.

Regarding the Appellant arguments that "the problem to be solved" by the present invention e.g. providing a direct communication between a memory module and a processor of the electronic device using a fast non-volatile random access memory". The problem to be solved " proving direct communication between a memory module and a processor" as argued, is inherently provided by the memory connecting to the processor using the DDR interface as taught by Lin's column 4 lines 35-39, Fig 1: #74. Lin further teaches a fast efficiently method to

store data into DDR memory in a permanent manner, thus making the memory become a fast non-volatile access memory and thereby further providing data quickly to the DDR interface for communication with the processor. One skill in the art would recognize Lin's teaching of DDR interface and fast non-volatile random access memory and include into Ganton's system thereby providing a fast accessing memory subsystem. Therefore Appellant's arguments are not persuasive.

B) Regarding claims 20 and 33, the arguments are similar to the arguments offered for claim 1 and the same responses apply. Additionally, Appellant merely alleges the motivation of combine teaching of recited prior art, and failing to point out any specific issue with the combined teaching as stated in the rejections of these claims. As such, these arguments are found to be not persuasive.

C) Appellant arguments regarding the rejections of claims 2 and 12 under 35 USC 103(a) are not persuasive. The arguments are similar to the arguments offered for claim 1 and the same responses apply (item A above) . Additionally, Appellant merely alleges the motivation of combine teaching of recited prior art, and failing to point out any specific issue with the combined teaching as stated in the rejections of these claims. As such, these arguments are found to be not persuasive.

D) Appellant's arguments regarding the rejections of depending claims 3-4, 8, 21-22 under 35 USC 103(a) are not persuasive for reasons similar to those set forth above with respect to the patentability of the independent claims 1 and 20. Additionally, Appellant merely alleges the motivation of combine teaching of recited prior art, and failing to point out any specific issue

with the combined teaching as stated in the rejections of these claims. As such, these arguments are found to be not persuasive.

E) Appellant's arguments regarding the rejections of depending claims 5 and 7 under 35 USC 103(a) are not persuasive for reasons similar to those set forth above with respect to the patentability of the dependent claim 4. Moreover, Appellant repeats the same argument about the "non-volatile random access memory" which Examiner addressed in item A above. Additionally, Appellant merely alleges the motivation of combine teaching of recited prior art, and failing to point out any specific issue with the combined teaching as stated in the rejections of these claims. Additionally, Appellant alleges that Witek does not teach the limitation of claim 7, rather than actual arguments with respect to the claimed subject matter and Witek disclosure.

As such, these arguments are found to be not persuasive.

F) Regarding claim 6, Appellant repeats the same argument that he made with respect to claim 5. The Board's attention is respectfully directed to response to these arguments in item E above.

G) Regarding claims 9-11, 13-18 and 34, the arguments are similar to the arguments offered for claim 1 and the same responses apply. Appellant further argues that "Pua et al disclose the non-volatile memory storage integrated circuit 10 (see par. 20, lines 4-6) and does not contain "mass" memory which is further evident from the description of Pua et al. : to easily extend the capacity of the, by merely connecting the terminal corresponding to the SRAM IC 1411 to the desired memory terminal..". Examiner disagrees. The "mass"' memory is a bulk memory to provide additional memory thus easily extending the capacity of the overall memory in the system. This definition is supported by The Authoritative Dictionary Of IEEE Standards

Terms Seventh Edition, which states "bulk storage A supplement large volume memory or storage device". Thus Pua clearly teaches that this additional memory can be easily attached to the SRAM IC 1411, thus easily extending the overall memory capacity in the system. Therefore Pua teaches that the integrate circuit package Fig 2 including several IC (integrate circuit) such as Fig 2 controlling IC, SRAM memory IC and bulk memory IC attaching to the terminal 1411 which corresponds to the claim's "mass memory".

Additionally, Appellant merely alleges the motivation of combine teaching of recited prior art, and failing to point out any specific issue with the combined teaching as stated in the rejections of these claims.

As such, these arguments are found to be not persuasive.

H) Regarding claim 19, The arguments are similar to the arguments offered for claim 1 and the same responses apply (item A above) .

Additionally, Appellant merely alleges the motivation of combine teaching of recited prior art, and failing to point out any specific issue with the combined teaching as stated in the rejections of these claims.

As such, these arguments are found to be not persuasive.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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Duc T. Doan
Examiner
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Conferees:

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Attachment:

IEEE 100 The Authoritative Dictionary of IEEE Standards Terms Seventh Edition 2000.

Microsoft Computer Dictionary Fifth Edition 2002